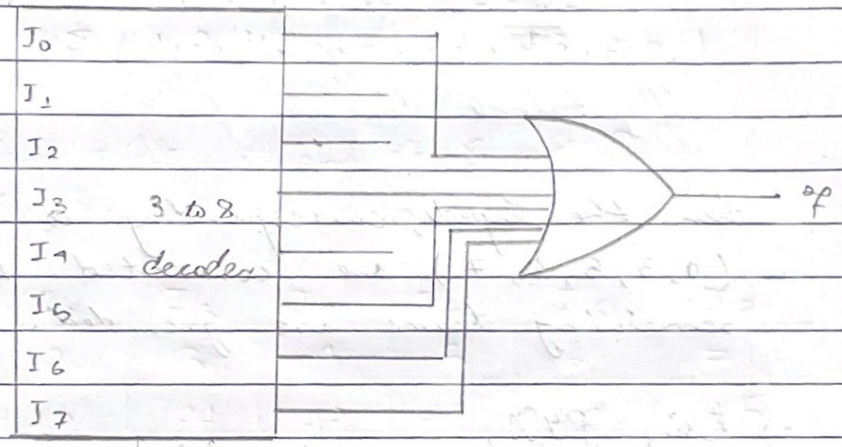
Combinational Logic with MUX and DMUX.

1. Implement the following function $F = \Sigma(0, 3, 5, 6, 7)$ (2074)
a) Decoder. b) Multiplexer c) PLA.

Solution:

$$F(A, B, C) = \Sigma(0, 3, 5, 6, 7)$$

a) Here, the function has 3 inputs (A, B, C) and 8 outputs. So, we'll use 3:8 decoder to implement this function.



b) Using multiplexer:

Let $F(A, B, C) = \Sigma(0, 3, 5, 6, 7)$

Here, it has to be 3 inputs and 8×1 MUX should be implemented.

Let S_0, S_1, S_2 be three status lines.

Implementation table:

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	0	1	2	3	4	5	6	7
A	8	9						
	1	0	0	1	0	1	1	1

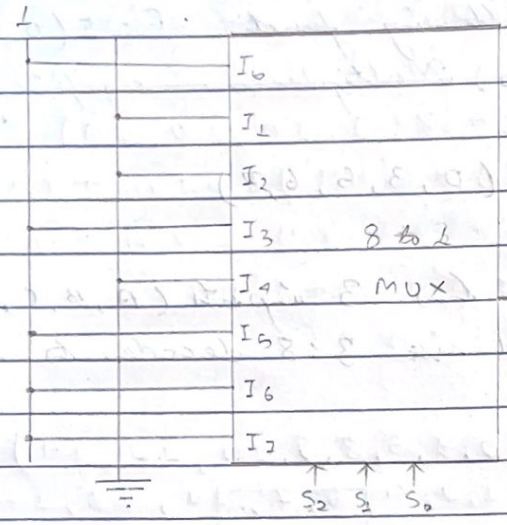


Fig. Block diagram of 8 to 1 Multiplexer

here, the inputs corresponding to min terms (0, 3, 5, 6, 7) are connected to 1 and the remaining terms are grounded.

c) Using PYA,

$F = \Sigma(0, 3, 5, 6, 7)$

K map for given function:

A\BC	00	01	11	10
0	1	0	1	0
1	0	1	1	1

~~True = x'y'z' + xz~~

True = A'B'C' + AC + AB + BC

Compliment = AB'C' + A'B'C + A'BC'

here, No. of input buffers = no. of variable
= 3 (i.e. A, B, C)

No. of programmable AND gate
= No. of min terms
= 4.

No. of programmable OR gate:
= No. of output functions.
= 1.